

## Methods of Technical Implementation of Receivers of Systems for Monitoring The State of Rail Lines for Railways Uzbekistan

Azamat Nematullayevich Sadikov  
Tashkent State Transport University

\*\*\*

### Annotation

The issues of improving the system for monitoring the state of rail lines with the transfer of technical means to a modern, more reliable microelectronic base are considered. Using the methods of detecting the disorder of random processes and linear filtering, the algorithm of the detector of signals for monitoring the state of rail lines is implemented. The considered algorithm of the receiver of the system for monitoring the states of the rail line can be practically implemented on a microprocessor-based element base.

**Key words:** monitoring the state of rail lines, microprocessor element base, microprograms, timer, receiver, signal, band pass filter

### Introduction

Further improvement of the system for monitoring the state of rail lines (MRL) is associated with the transfer of technical means to a modern, more reliable microelectronic base. This will expand their functionality, reduce the energy and material consumption of the equipment. The use of new, more advanced algorithms for the processing of signals from the MRL, the implementation of which on the old element base was fundamentally impossible [1].

Using the methods of detecting the disorder of random processes and linear filtering, an algorithm for the operation of the detector of signals MRL is implemented. In order to determine the characteristics of noise immunity and false detection of control signals, statistical modeling of the considered algorithm of the MRL receiver operation was carried out. The results of statistical modeling of the MRL receiver operation algorithm confirmed its high operational and technical indicators. [2,3].

### Material and Methods

The considered algorithm of the receiver of the system for monitoring the states of the rail line can be practically implemented on a microprocessor-based element base. Thanks to the use of modern methods of processing useful signals, the receiver will ensure the detection of a useful signal at low signal-to-noise ratios. An electromechanical relay serves as an actuating element of the MRL system receiver, the contacts of which are used in relay path blocking circuits [4,5].

Mass-produced industrial microprocessors are divided into two groups:

- with firmware control;
- with a fixed (standard) set of commands.

The first group includes microprocessors of the K588 and K1804 series. They have the ability to increase the bit depth of the address and data buses, have a high data processing speed, but require the development of specialized software, which increases the range of components of the microprocessor controller.

The second group includes microprocessors of the K580, K1810 and K1821 series. The microprocessors of these series are made on the basis of a single chip. For these microprocessors, there is a wide range of different peripheral chips. The programming process of these microprocessors is characterized by simple execution. All microprocessors of the second group are software compatible, which ensures the continuity of the software.

The complexity of developing specialized microcomputers for receiving devices of MRL systems based on microprocessors with a fixed set of commands is significantly easier than when using a firmware series [6].

From the microprocessors of the second group, we choose the most rational one for building a receiver of the MRL system.

As the selection criteria, we consider the following:

- data bus bit rate;
- performance;
- address memory capacity;
- power consumption;
- nomenclature of supply voltages;

The K580VM80 microprocessor is currently the most common. The nomenclature of Large Integrated Circuits in the kit has an eight-bit data bus. The main drawback is the need for three power sources +5V, +12V and -5V. The K580VM80 microprocessor has a low speed, about 2 microseconds. The power consumption is 1.5 W [7].

The K1810VM86 microprocessor has a performance 4 times higher than the K580VM80 (0.5 microseconds). The K1810VM86 chip uses a sixteen-bit data bus. The disadvantage of this microprocessor is the high power consumption-about 1.75 W, which makes its use in the MRL system economically impractical.

The K1821VM85 microprocessor is on a par with the K580VM80 and K1810VM86 microprocessors considered in terms of performance (0.8 microseconds). In terms of power consumption, it significantly exceeds the chips discussed above. At the software level, the K1821VM85 microprocessor is fully compatible with the K580VM80 microprocessor, which makes the programs developed for the K580VM80 series microprocessor compatible.

Thus, when developing a microprocessor-based track receiver (MTR) of the MRL system, it is advisable to focus on the K1821VM85 microprocessor kit [8,9].

The structure of a specialized microcomputer for the receiver of the MRL system is determined by the type of microprocessor used and the level of tasks solved by the microcomputer. When using the K1821VM85 microprocessor, signals are generated on the address, data and control buses using the K580BA86 and

K580IR82 chips. The amount of memory required is determined based on the following tasks:

- control signal reception and processing;
- deciding on the state of the rail line;
- control of time parameters of code combinations;
- monitoring the health of the threads of the traffic light channel.

To solve the control program of the receiver of the MRL system, the memory capacity is 16 kbytes [10,11].

To organize the input-output of information and control signals, the microprocessor controller provides 12 inputs and outputs. Eight inputs are used to enter information and an analog-to-digital converter, 4 inputs are used to control the operating mode of the microcomputer. Twelve outputs are used to control the information input processor, test the input-output device and link with the station interlocking system device. For this purpose, a parallel programmable adapter K580BB55 is used, which contains three bidirectional eight-bit ports.

The block diagram of a specialized microcomputer is shown in Fig. 1. In order to reduce the number of peripheral microcircuits, the ROM program memory is made on two K573RF4 elements with a volume of 8 KB. The random access memory of the RAM is made on one static type microcircuit K537RU10 with a capacity of 2 KB.

The microprocessor, ROM, RAM, and I / O port are combined by a sixteen-bit address bus. Information is exchanged over the data bus between the timer, the microprocessor, ROM, RAM and the I / O port. In addition, the data bus is used in the operation of the signature analyzer. In the signature analyzer, the input signals are folded and the control signals of KT and  $\overline{KT}$  are formed. Chips ROM, RAM, I / O port, timer and microprocessor are combined by a read bus -  $\overline{RD}$  and write -  $\overline{WR}$  signals.

**Results and Discussion**

The MTR receiver is made according to a two-set scheme with rigid synchronization (Fig. 2). Each kit contains CPU modules CP1, CP2 and SA signature analyzers. The control of the correct functioning of the MTR is carried out by a single-stage control circuit of the CC. The initial start of the receiver and the synchronization of CP1 and CP2 performs the start process SP. The input circuits of the receiver contain: a bandpass filter BF, an envelope detector D, an integrator I and an analog-to-digital converter ADC.

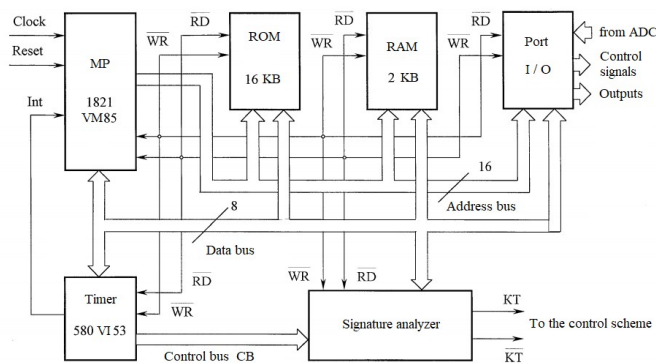


Fig. 1. Block diagram of a specialized microcomputer

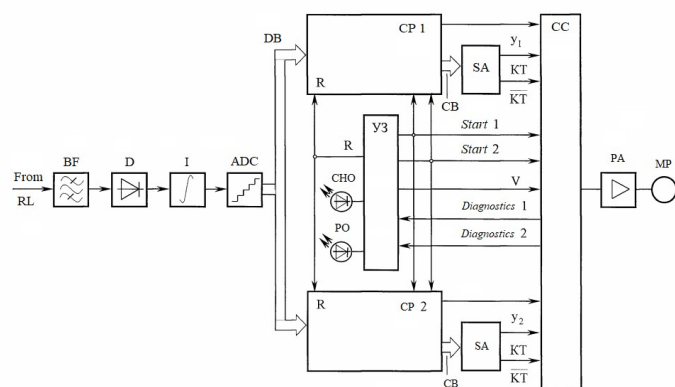


Fig. 2. Block diagram of the microprocessor track receiver of the MRL system

Consider the operation of the receiver. The useful signal from the output of the rail line through the BF bandpass filter enters the envelope detector D, where it is rectified, smoothed in the integrator I and then,

using an analog-to-digital converter, the ADC is quantized in amplitude and sampled in time.

The value of the signal in the binary formula via the data bus of the DB is fed to the input-output ports of the CP1, CP2 nodes of both sets. The received data is processed in accordance with the algorithm stored in the ROM. If, after performing the calculations, the value of the decisive statistics exceeds the threshold, then control voltage pulses appear on the buses, which open the inputs of the control system. In this case, the control signal V with a frequency of 89.9 Hz from the output of the launch node is fed through the SC to the PA power amplifier to turn on the MP relay. If the cumulative sum does not exceed the threshold, then there are no signals at the outputs and the MP relay armature is released.

During the normal operation of the receiver, text signals are sent from the control points of the CP1 and CP2 nodes via the CB control buses to the circuit of the SA signature analyzer. SA generates common control signals  $y_1, y_2$  and  $KT, \overline{KT}$ , which characterize the performance of CP1 and CP2 nodes. If the signal forms  $y_1, y_2$  and  $KT, \overline{KT}$ , AA coincide, then the control circuit records the correct operation of the sets. The glow of the indicator LEDs of the CHO and PO indicates the serviceable condition of the receiver. Otherwise, a failure is recorded. At the outputs Diagnostics 1 and Diagnostics 2, control pulses appear that affect the ultrasonic start node, which, with a given time delay, generates control pulses Start 1 and Start 2 to restore the working state of the receiver sets. If, as a result of the influence of these pulses, the normal functioning of the receiver is restored, then the control signals Diagnostics 1 and Diagnostics 2 are removed. Otherwise, when the failure in one of the channels of the receiver is stable and the recovery of the functional state of the receiver does not occur, the PC protection cell counts eight start pulses and stops. The receiver switches to a stable safe failure position.

**Conclusion**

When the power is turned on for the first time, as well as after power supply interruptions, the working state

of the receiver is restored by the start node on the Start 1 and Start 2 buses. After switching on the voltage on these buses, a pulse sequence appears that sets the microprocessor sets of CP1 and CP2 nodes to their initial state. From this moment, the normal operation of the MTR receiver begins.

Structurally, the microprocessor track receiver is made of a single metal block. Removable components are placed on the frame of the unit, which can be easily replaced during operation. The nomenclature of a typical MTR replacement element is as follows: a central processor node and launch cells, a control circuit node, a power source and a bandpass filter.

## References

1. Belyakov IV Theory and methods of implementation of adaptive systems for monitoring the states of rail lines: Diss ... doct. tech. Sciences: 05.22.08 / MSU PS (MIIT) .- M., 1996, - 441 p.
2. Belyakov IV, Kraskovsky AE, Razumovskaya EA Detection of changes in signal parameters when controlling railway traffic lights // Statistical problems of control: Methods for recognizing random processes.-Vilnius, 1990.-Issue 89.-C ... 25-31.
3. Le Thi Van Anh. Microprocessor-based haulage control system for sections with semi-automatic blocking. Diss. Cand. tech. sciences.
4. Kraskovsky AE Nonlinear filtering and optimal reception of delayed signals: Textbook. Benefit. - L. , 1985, - 120 p.
5. Belyakov IV Monitoring of the states of rail lines in the presence of interference from traction current: Diss. Cand. those. Sciences: 05.22.08 / MIIT, - M., 1988.-262 p.
6. Nikiforov IV Sequential detection of changes in properties, time series.-Moscow: Nauka, 1983, - 200 p.
7. Aripov N.M., Rikhsiev D.Kh. Microprocessor technologies in railway automation and telemechanics systems // International scientific and practical conference "EurasiaScience". Moscow, October 31, 2018.
8. Aripov N., Aliyev R., Baratov D.X., Ametova E.K. Features of construction of systems of railway automatics and telemechanics at the organization of high-speed traffic in the republic of Uzbekistan. // 9th international scientific conference Transbaltica 2015/ Vilnius, 7–8 may, 2015. Procedia Engineering 134 (2016) P. 175 – 180.
9. Azizov A.R., Sadikov A.N. Development of a scheme for linking a microprocessor pulse relay with existing systems of railway automation and telemechanics. Republican scientific and technical conference with the participation of foreign scientists "Resource-saving technologies of automation, electrical communication and power supply of railway transport." - Tashkent, TashIIT. 2017. - pp. 176-178.
10. Azizov A.R., Yuldashev Sh.M., Sadikov A.N. Modeling and optimization of the operation algorithm of an electromechanical impulse relay. // Bulletin of transport of the Volga region, November-December 2018. No. 4.
11. N. Aripov, A. Sadikov, S. Ubaydullayev. Intelligent signal detectors with random moment of appearance in rail lines monitoring systems. // E3S Web of Conferences 264, 05039 (2021). CONMECHYDRO – 2021
12. D.I. Mamurova. The role of graphics programs in improving the learning process using information technology. EFFLATOUNIA-Multidisciplinary Journal 5 (2)
13. Aminov, A. S., Mamurova, D. I., & Shukurov, A. R. (2021, February). ADDITIONAL AND DIDACTIC GAME TECHNOLOGIES ON THE TOPIC OF LOCAL APPEARANCE. In *E-Conference Globe* (pp. 34-37).
14. Islamovna M. D., Gulhumor M. PRINCIPLE OF TEACHING DRAFT GEOMETRY AND COMPUTER GRAPHICS //World Bulletin of Social Sciences. – 2020. – T. 1. – №. 1. – C. 30-31.